We claim:

1. A printed circuit board configuration with a multipole plug-in connector, comprising:

a board having at least two layers, each one of said at least two layers having an edge region;

a plurality of signal conductor tracks disposed in said edge region of one of said layers;

a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;

a plurality of ground conductor tracks disposed on said one of said layers and assigned to said plurality of said signal conductor tracks;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternatingly disposed on said one of said layers, and in which said plurality of said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor tracks; and

a ground shielding surface disposed on an adjacent one of said layers and covering said side-to-side configuration.

2. The printed circuit board configuration according to claim 1, wherein said board is formed with a plurality of plated through-holes therein, and said plurality of said plated through-holes electrically connect said plurality of said ground conductor tracks to said ground shielding surface.

3. The printed circuit board configuration according to claim 2, wherein each one of said plurality of said ground conductor tracks is electrically connected to said ground shielding surface by more than one of said plurality of said plated-through holes.

4. The printed circuit board configuration according to claim 1, wherein said at least one filter capacitor includes a plurality of filter capacitors, each one of said plurality of said filter capacitors connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor

tracks at a location remote from said plurality of said plug pins.

5. The printed circuit board configuration according to claim 1, comprising a shielding plate covering said side-to-side configuration, said side-to-side configuration defining a first surface adjacent said ground shielding surface and defining a second surface that is opposite said first surface and that is adjacent said shielding plate.

6. The printed circuit board configuration according to claim 5, wherein said plurality of said ground conductor tracks includes two outer ground conductor tracks, and said shielding plate is fixed on and electrically connected to said two outer ground conductor tracks.

7. The printed circuit board configuration according to claim 1, wherein:

said one of said layers defines a first outer board layer, said another one of said layers defines an inner board layer, said at least two layers includes a second outer board layer remote from said first outer board layer, said second outer board layer has an outer edge region; and

said plurality of said signal conductor tracks defines a first plurality of signal conductor tracks, said plurality of said plug pins defines a first plurality of plug pins, said plurality of said ground conductor tracks defines a first plurality of ground conductor tracks, and said side-to-side configuration defines a first side-to-side configuration, the printed circuit board configuration including:

a second plurality of signal conductor tracks disposed in said edge region of said second outer board layer;

a second plurality of plug pins, each one of said second plurality of said plug pins fixed to a respective one of said second plurality of said signal conductor tracks in a direction parallel to said second outer board layer;

a second plurality of ground conductor tracks disposed on said second outer board layer and assigned to said second plurality of said signal conductor tracks; and

a second side-to-side configuration in which said second plurality of said signal conductor tracks and said second plurality of said ground conductor tracks are alternatingly disposed on said second outer board layer, and in which said second plurality of said signal conductor tracks run

essentially parallel with respect to said second plurality of said ground conductor tracks.